

Appl. No. : 09/808,612  
Filed : March 14, 2001

**IN THE SPECIFICATION**

1. On Page 4, lines 10-11 of the specification as filed, please amend the text as follows:

5

-- Fig. 1 is a logical flow diagram illustrating one exemplary embodiment of the general debugging methodology employed by the present invention. --

2. On Page 3, lines 22-27 of the specification as filed, please amend the text as follows:

10

-- In a third aspect of the invention, an improved debug architecture is disclosed. In one exemplary embodiment, the improved debug architecture comprises a digital processor with a debug process running thereon, at least one simulation process associated and in data communication therewith, and at least one hardware process in data communication with the processor, wherein the simulation and hardware processes are executed with a single thread of control via the ~~debug~~ debug process. --

15